

AMENDMENTS TO THE CLAIMS

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

Listing of Claims:

1. (Currently Amended) A method of fabricating a SOI substrate, comprising:

sequentially forming a first semiconductor layer, a second semiconductor layer and a buried oxide layer on a front surface of a semiconductor substrate;

forming a buffer oxide layer on a front surface of a supporting substrate;

forming an etch stopping layer on ~~a front surface of a supporting substrate~~ the buffer oxide layer;

contacting the etch stopping layer with the buried oxide layer to bond the semiconductor substrate to the supporting substrate; and

selectively removing the semiconductor substrate and the first semiconductor layer to expose the second semiconductor layer.

2. (Currently Amended) ~~The method as claimed in claim 1, wherein the first semiconductor layer~~

A method of fabricating a SOI substrate, comprising:

sequentially forming a first semiconductor layer, which is a porous semiconductor epitaxial layer, a second semiconductor layer and a buried oxide layer on a front surface of a semiconductor substrate;

forming an etch stopping layer on a front surface of a supporting substrate;

contacting the etch stopping layer with the buried oxide layer to bond the semiconductor substrate to the supporting substrate; and  
selectively removing the semiconductor substrate and the first semiconductor layer to expose the second semiconductor layer.

3. (Currently Amended) ~~The method as claimed in claim 1, wherein the etch stopping layer~~

A method of fabricating a SOI substrate, comprising:  
sequentially forming a first semiconductor layer, a second semiconductor layer and a buried oxide layer on a front surface of a semiconductor substrate;  
forming an etch stopping layer, which is formed of a silicon nitride layer on a front surface of a supporting substrate;  
contacting the etch stopping layer with the buried oxide layer to bond the semiconductor substrate to the supporting substrate; and  
selectively removing the semiconductor substrate and the first semiconductor layer to expose the second semiconductor layer.

4. (Currently Amended) ~~The method as claimed in claim 1, wherein the first semiconductor layer~~

A method of fabricating a SOI substrate, comprising:  
sequentially forming a first semiconductor layer, which is a bubble layer, a second semiconductor layer and a buried oxide layer on a front surface of a semiconductor substrate;

forming an etch stopping layer on a front surface of a supporting substrate;  
contacting the etch stopping layer with the buried oxide layer to bond the  
semiconductor substrate to the supporting substrate; and  
selectively removing the semiconductor substrate and the first semiconductor  
layer to expose the second semiconductor layer.

5. (Canceled)

6. (Original) A method of fabricating a SOI integrated circuit, comprising:  
preparing a SOI substrate having a first conductivity type supporting substrate,  
an etch stopping layer stacked on the supporting substrate, a buried oxide layer stacked  
on the etch stopping layer, and a semiconductor layer stacked on the buried oxide layer;  
forming a device isolation layer at a predetermined region of the semiconductor  
layer to define first and second active regions;  
continuously dry-etching the device isolation layer and the buried oxide layer to form  
first and second preliminary holes exposing the etch stopping layer;  
wet-etching the etch stopping layer exposed by the first and second preliminary  
holes to form first and second holes exposing the supporting substrate;  
growing first and second semiconductor epitaxial layers in the first and second  
holes, respectively;  
forming first and second conductivity type pick-up regions at the surfaces of the  
first and second semiconductor epitaxial layers, respectively; and

forming NMOS and PMOS transistors at the first and second active regions, respectively.

7. (Original) The method as claimed in claim 6, wherein the first and second conductivity types are p-type and n-type, respectively.

8. (Original) The method as claimed in claim 7, wherein the first conductivity type pick-up region is simultaneously formed with source/drain regions of the PMOS transistor, and the second conductivity type pick-up region is simultaneously formed with source/drain regions of the NMOS transistor.

9. (Original) The method as claimed in claim 6, wherein the first and second conductivity types are n-type and p-type, respectively.

10. (Original) The method as claimed in claim 9, wherein the first conductivity type pick-up region is simultaneously formed with source/drain regions of the NMOS transistor, and the second conductivity type pick-up region is simultaneously formed with source/drain regions of the PMOS transistor.

11. (Original) The method as claimed in claim 6, wherein the etch stopping layer is formed of a material layer having an etch selectivity with respect to the buried oxide layer and the device isolation layer.

12. (Original) The method as claimed in claim 11, wherein the etch stopping layer is formed of a silicon nitride layer.

13. (Original) The method as claimed in claim 6, further comprising forming a buffer oxide layer between the supporting substrate and the etch stopping layer, wherein the first and second holes are formed by continuously wet-etching the etch stopping layer and the buffer oxide layer.

14. (Original) The method as claimed in claim 6, further comprising selectively forming a metal silicide layer on the pick-up regions, a gate electrode and source/drain regions of the NMOS transistors, and a gate electrode and source/drain regions of the PMOS transistors.

15. (Original) The method as claimed in claim 7, further comprising:  
forming an interlayer insulation layer on the entire surface of the resultant structure where the NMOS and PMOS transistors are formed; and  
forming a first interconnection electrically connected with the first conductivity type pick-up region and a second interconnection electrically connected with the second conductivity type pick-up region on the interlayer insulation layer.

16. (Original) The method as claimed in claim 15, further comprising forming an input pad connected with the second interconnection on the interlayer insulation layer,

wherein the second interconnection is electrically connected with the gate electrodes of the NMOS and PMOS transistors.

17. (Original) A method of fabricating a SOI integrated circuit, comprising:  
preparing a SOI substrate having a first conductivity type supporting substrate, an etch stopping layer stacked on the supporting substrate, a buried oxide layer stacked on the etch stopping layer, and a semiconductor layer stacked on the buried oxide layer;  
forming a device isolation layer at a predetermined region of the semiconductor layer to define first and second active regions;  
continuously dry-etching the device isolation layer and the buried oxide layer to form first and second preliminary holes exposing the etch stopping layer;  
forming a first conductivity type pick-up region at the supporting substrate below the etch stopping layer exposed by the first preliminary hole;  
forming a second conductivity type pick-up region at the supporting substrate below the etch stopping layer exposed by the second preliminary hole; and  
forming NMOS and PMOS transistors at the first and second active regions, respectively.

18. (Original) The method as claimed in claim 17, wherein the first and second conductivity types are p-type and n-type, respectively.

19. (Original) The method as claimed in claim 17, wherein the first and second conductivity types are n-type and p-type, respectively.

20. (Original) The method as claimed in claim 17, wherein the etch stopping layer is formed of a material layer having an etch selectivity with respect to the buried oxide layer and the device isolation layer.

21. (Original) The method as claimed in claim 20, wherein the etch stopping layer is formed of a silicon nitride layer.

22. (Original) The method as claimed in claim 17, further comprising forming a buffer oxide layer between the supporting substrate and the etch stopping layer.

23. (Original) The method as claimed in claim 17, further comprising selectively forming a metal silicide layer on the first conductivity type pick-up region, the second conductivity type pick-up region, a gate electrode and source/drain regions of the NMOS transistors, and a gate electrode and source/drain regions of the PMOS transistors.

24. (Original) The method as claimed in claim 18, further comprising:  
forming an interlayer insulation layer on the entire surface of the resultant structure where the NMOS and PMOS transistors are formed; and

forming a first interconnection electrically connected with the first conductivity type pick-up region and a second interconnection electrically connected with the second conductivity type pick-up region on the interlayer insulation layer.

25. (Original) The method as claimed in claim 24, further comprising forming an input pad connected with the second interconnection on the interlayer insulation layer, wherein the second interconnection is electrically connected with the gate electrodes of the NMOS and PMOS transistors.

Claims 26-41. (Canceled)